

MCHSTREAMER

MULTI-CHANNEL MULTI-PROTOCOL USB AUDIO INTERFACE

User Manual

TOSLINK

S/PDIF

I2S

DSD

ADAT

TDM

PDM





Revision history

Revision	Description	Date
1.0	First public release	8 March 2019
1.0a	Added 3 rd party logos	2 July 2019
1.1	Modifying pin out for DSD mode	26 Aug 2019

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IMPORTANT INFORMATION

Please read the following information before use. In case of any questions, please contact miniDSP via the support portal at minidsp.desk.com.

SYSTEM REQUIREMENTS — WINDOWS

- 1GHz or higher processor clock speed recommended / Intel® Pentium®/Celeron® family, or AMD K6®/AMD Athlon®/AMD Duron® family, or compatible processor recommended.
- 512 megabytes (MB) of RAM or higher recommended
- One free USB 2.0 port
- Microsoft® Windows® XP SP2/Vista/Win7/Win8/Win10

SYSTEM REQUIREMENTS — MAC OS X

- Intel Core Duo processor or greater
- 256 megabytes (MB) of RAM or higher recommended
- One free USB 2.0 port
- Mac OS X 10.8 or greater

DISCLAIMER/WARNING

miniDSP cannot be held responsible for any damage that may result from the improper use or incorrect configuration of this product. Please read this manual carefully to ensure that you fully understand how to operate and use this product, as incorrect use or use beyond the parameters and ways recommended in this manual have the potential to cause damage to your audio system.

Please also note that many of the questions we receive at the technical support department are already answered in this User Manual and in the online [application notes](#) on the miniDSP.com website. So please take the time to carefully read this user manual and the online technical documentation. Thank you for your understanding!

WARRANTY TERMS

miniDSP Ltd warrants this product to be free from defects in materials and workmanship for a period of one year from the invoice date. Our warranty does not cover failure of the product due to incorrect connection or installation, improper or undocumented use, unauthorized servicing, modification or alteration of the unit in any way, or any usage outside of that recommended in this manual. If in doubt, contact miniDSP prior to use.

FCC CLASS B STATEMENT

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.



Warning: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Notice: Shielded interface cable must be used in order to comply with emission limits.

Notice: Changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

CE MARK STATEMENT

The MCHStreamer has passed the test performed according to European Standard EN 55022 Class B.

A NOTE ON THIS MANUAL

This User Manual is designed for reading in both print and on the computer. If printing the manual, please print double-sided. The embedded page size is 8 1/2" x 11". Printing on A4 paper will result in a slightly reduced size.

For reading on the computer, we have included hyperlinked cross-references throughout the manual. In addition, a table of contents is embedded in the PDF file. Displaying this table of contents will make navigation much easier:

- In Adobe Reader on Windows, click on the "bookmarks" icon at the left. The table of contents will appear on the left and can be unfolded at each level by clicking on the "+" icons.
- In Preview on the Mac, click on the **View** menu and select **Table of Contents**. The table of contents will appear on the left and can be unfolded at each level by clicking on the triangle icons.



1 PRODUCT OVERVIEW

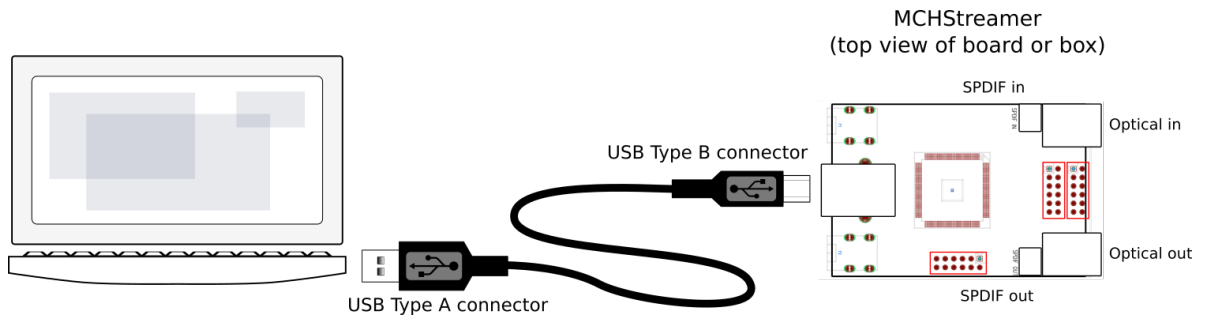
Thank you for purchasing a miniDSP *MCHStreamer* USB audio interface. The MCHStreamer comes in two versions: kit and boxed. The boxed version has a pair of optical ports that can be used for TOSLINK or ADAT I/O while the kit version additionally supports headers for logical-level I/O data formats: I2S, TDM, PDM, and DSD.

- TOSLINK optical stereo in and out, 44.1 to 192 kHz
- SPDIF stereo in and out, 44.1 to 192 kHz
- ADAT 8-channel in and out (44.1 and 48 kHz), 4-channel in and out (88.2 and 96 kHz), with automatic conversion to logic-level I2S
- I2S 8-channel in and out, 8 kHz to 384 kHz
- DSD stereo and 8-channel out at DSD64, DSD128 and DSD256
- TDM input and output up to 96 kHz, up to 24 channels
- PDM 16-channel input with automatic conversion to logic-level I2S

2 CONNECTIVITY

2.1 USB

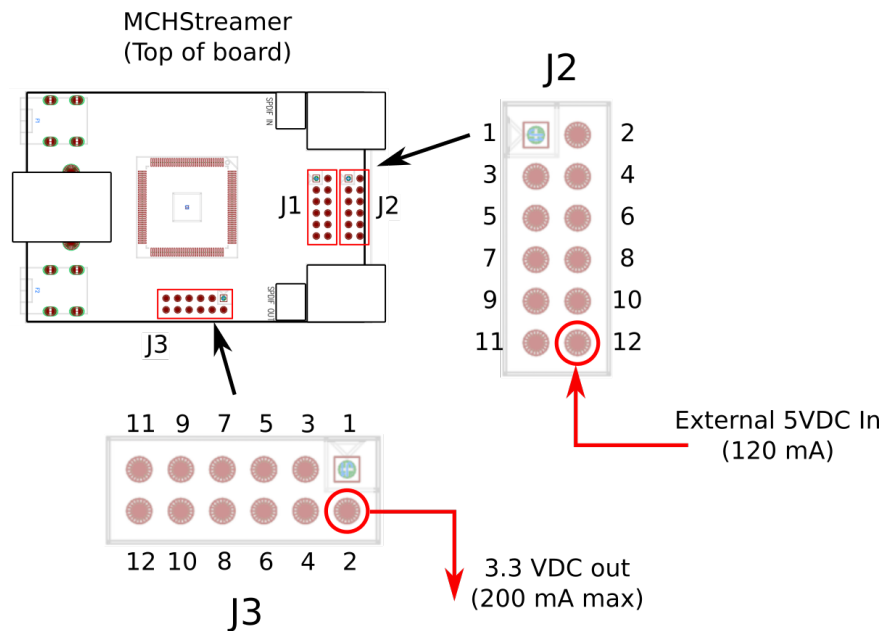
Connect as shown (for either box or kit version). The USB port provides power and computer connectivity.



2.2 EXTERNAL POWER

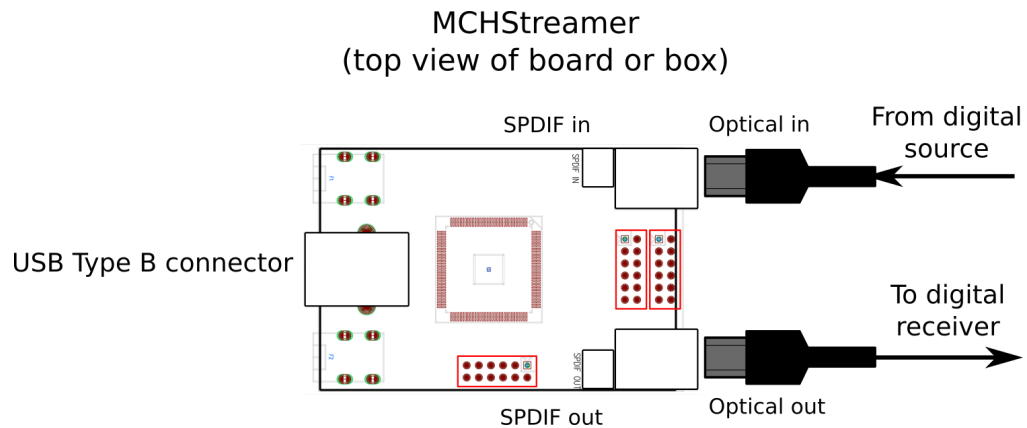
External 5V DC power can be connected to the MCHStreamer via pin 12 of J2. This pin is connected with a “diode-or” connection to the power line from the USB port. Supplying 5V DC to this pin will therefore ensure that the MCHStreamer remains powered on even when no USB device is connected. The MCHStreamer consumes no more than 120 mA from this pin, plus any additional current draw required for pin 2 of J3.

The MCHStreamer can supply external circuitry with 3.3 V from pin 2 of J3. The maximum current draw allowed on this pin is 200 mA.



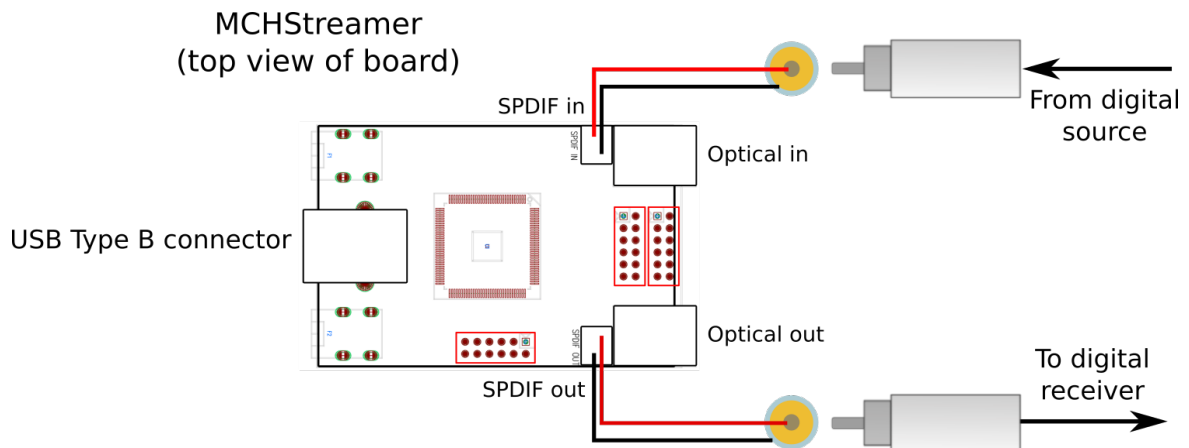
2.3 OPTICAL

The optical port supports SPDIF or ADAT, depending on the firmware loaded.



2.4 SPDIF

The SPDIF I/O is accessed with a pair of two-pin headers adjacent to the optical ports. These are normal consumer-level (0.5V) lines, so additional circuitry for level shifting is not required. Note however that these lines are not galvanically isolated.



2.5 LOGIC-LEVEL I/O

2.5.1 Overview

In addition to the optical and SPDIF interfaces described above, the MCHStreamer provides a wealth of different data formats as logic-level signals:

- I2S, or Inter-IC Sound, is used to carry PCM digital audio between digital chips (ICs) and circuit boards. The MCHStreamer circuit board provides up to 8 channels of I2S input and 8 channels of I2S output.
- TDM, or Time domain multiplexing, is a format used by some ADC and DAC chips to carry multiple channels on a single data line. This can reduce layout complexity and/or allow a greater number of channels.
- PDM, or Pulse density modulation, is commonly used by microphone arrays to efficiently carry a large number of channels at relatively low sample rates.
- DSD, or Direct Stream Digital (© Sony?), is a high-rate single-bit modulation and storage scheme that is used by some audiophile ADCs and DACs. It is used to play back DSD files.

Please note that logic-level connectivity is intended for professional engineers or **advanced** DIY users only. You will need the knowledge to understand digital clocking and wiring and have access to the equipment necessary to be able to debug any issues you may run into. (While miniDSP always tries to help its customers, it is infeasible for us to debug your circuit and wiring for you.)

Be sure to take the following precautions when designing your logic-level interface and wiring:

General usage notes

- Unbuffered lines must be kept short to ensure clock and data integrity.
- If driving longer lines, buffers may be required for the clock signals (MCLK, LRCLK, and BCLK).
- Observe correct grounding and shielding, and keep analog and digital grounds separated.
- Ensure that the clock ratios are compatible with connected circuits.

Clock master

The MCHStreamer always operates as clock master – that is, the clock lines are always outputs. The connected circuitry must therefore use the clocks provided by the MCHStreamer.

3.3V logic level

All lines use a 3.3V logic level. Ensure that connected circuits use a compatible level (1.8V, for example, will not work).

2.5.2 Headers and pinouts

The MCHStreamer circuit board has three 12-pin headers for logic-level I/O, as shown in Figure 1 below. Most data lines are on header J1, while J2 carries auxiliary signaling and GPIO lines reserved for future enhancement. J3 is used only for PDM format. Two cables terminated with suitable (2x6, 2mm pitch) 12-pin headers are supplied with the MCHStreamer kit version.

Table 1 lists the default pinouts. Note that these vary with the specific firmware loaded. See Section 3 for full details. All lines are 3.3V logic levels. Connected circuits must use a compatible logic level.

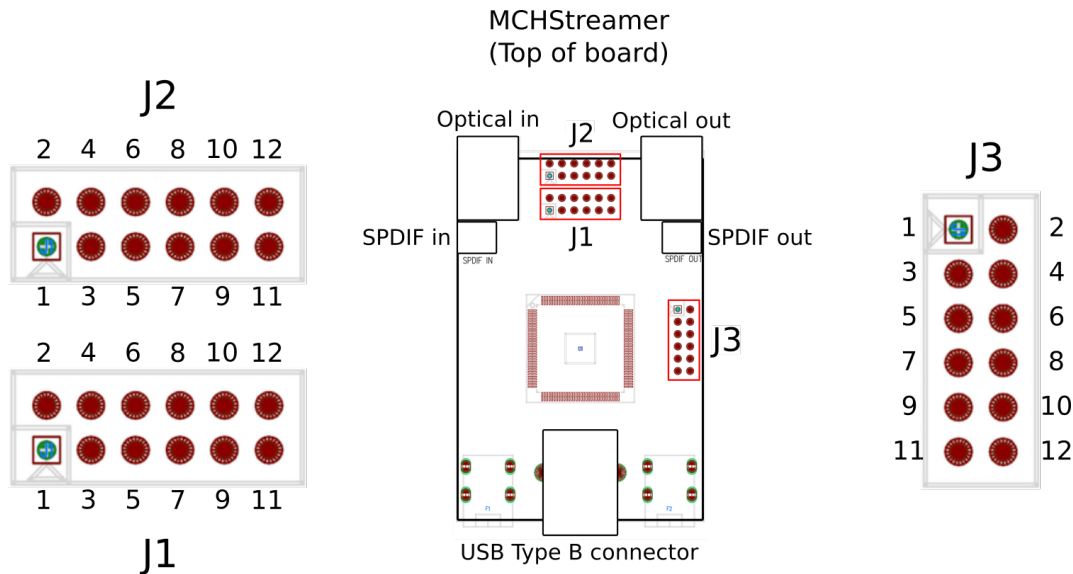


Figure 1. MCHStreamer board layout

Table 1. Sample pinouts (See Section 3 for details)

J1 (I2S mode only)		J2		J3	
Pin	Description	Pin	Description	Pin	Description
1	I2S data OUT Ch 1&2	1	Ground (GND)	1	GND
2	I2S data IN Ch 1&2	2	NC	2	3.3V
3	I2S data OUT Ch 3&4	3	Ground (GND)	3	PDM 1-2
4	I2S data IN Ch 3&4	4	NC	4	PDM 3-4
5	I2S data OUT Ch 5&6	5	NC	5	PDM 5-6
6	I2S data IN Ch 5&6	6	GPIO (future)	6	PDM 7-8
7	I2S data OUT Ch 7&8	7	GPIO (future)	7	PDM 9-10
8	I2S data IN Ch 7&8	8	RST (negative low)	8	PDM 11-12
9	Master clock (MCLK OUT)	9	GPIO (future)	9	PDM 13-14
10	Bit clock out (BCLK)	10	GPIO (future)	10	PDM 15-16
11	Ground (GND)	11	Ground (GND)	11	PDM CLK
12	I2S frame sync (LRCLK)	12	5V external power	12	PDM CLK2

2.5.3 I2S

2.5.3.1 Clocks

I2S has three clock lines. These clocks are always **outputs**. The connected circuitry must therefore be set to run in slave mode and accept its clocks from the MCHStreamer. (The MCHStreamer always runs as clock master; it cannot be set to run as a clock slave.)

- MCLK** The master clock for both playback and recording. This pin is always an output. Connected circuitry can choose whether or not to use it.
- LRCLK** The frame synchronization clock, also known as the word clock. This clock is equal to the sampling frequency (F_s) of the audio signal. This pin is always an output.
- BCLK** The bit clock (also known as shift clock or system clock). This is always equal to $64 \times F_s$. This pin is always an output.

Table 2 summarizes the relation between the clocks. Be sure to double-check that connected circuitry will accept the clocks at the frequencies and ratios listed.

Table 2. I2S clocks

Sample rate (LRCLK)	Master clock (MCLK)	Bit clock (BCLK)	MCLK/LRCLK	BCLK/LRCLK
8 kHz	24.576 MHz	512 kHz	3072	64
11.025 kHz	22.5792 MHz	705.6 kHz	2048	64
12 kHz	24.576 MHz	768 kHz	2048	64
16 kHz	24.576 MHz	1024 kHz	1536	64
32 kHz	24.576 MHz	2.048 MHz	768	64
44.1 kHz	22.5792 MHz	2.822 MHz	512	64
48 kHz	24.576 MHz	3.072 MHz	512	64
88.2 kHz	22.5792 MHz	5.6448 MHz	256	64
96 kHz	24.576 MHz	6.144 MHz	256	64
176.4 kHz	22.5792 MHz	11.2896 MHz	128	64
192 kHz	24.576 MHz	12.288 MHz	128	64
352.8 kHz	22.5792 MHz	22.5792 MHz	64	64
384 kHz	24.576 MHz	24.576 MHz	64	64

2.5.3.2 Timing

Each I2S data line carries two audio channels. There are up to four lines for input data and four lines for output data, depending on the firmware loaded. Input lines are always treated as 24-bit, while output lines can be 16-, 24- or 32-bit. The I2S data format and timing is shown in Figure 2 (only channels 1-4 shown).

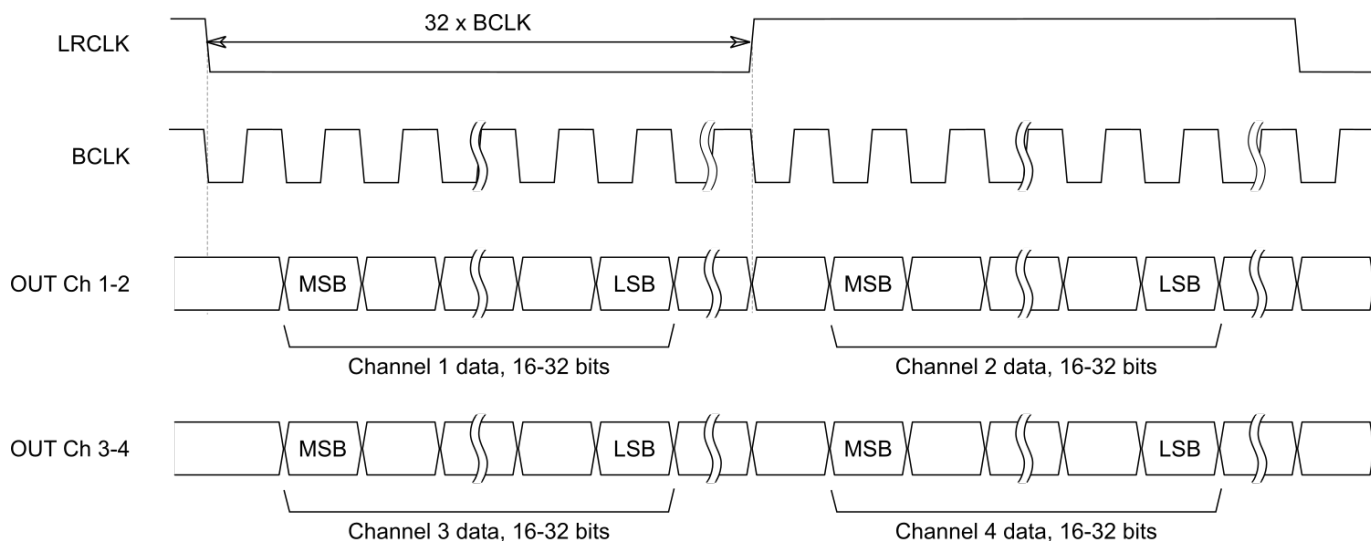


Figure 2. I2S timing

2.5.4 TDM

2.5.4.1 Clocks

TDM has three clock lines. These clocks are always **outputs**. The connected circuitry must therefore be set to run in slave mode and accept its clocks from the MCHStreamer. (The MCHStreamer cannot be set to run as a clock slave.)

- MCLK** The master clock for both playback and recording. This pin is an output only.
- FSYNC** The frame synchronization clock. This clock is equal to the sample rate and corresponds to eight 32-bit words. This pin is an output only.
- BCLK** The bit clock (also known as shift clock or system clock). This is always equal to $256 \times F_s$. This pin is an output only.

Table 3 summarizes the relation between the clocks. Be sure to double-check that connected circuitry will accept the clocks at the frequencies and ratios listed.

Table 3. TDM clocks

Sample rate	Frame Sync (FSYNC)	Master clock (MCLK)	Bit clock (SCLK)
44.1 kHz	44.1 kHz (one short)	22.5792 MHz	11.2896 MHz
48 kHz	48 kHz (one short)	24.576 MHz	12.288 MHz
88.2 kHz	88.2 kHz (one short)	22.5792 MHz	22.5792 MHz
96 kHz	96 kHz (one short)	24.576 MHz	24.576 MHz

2.5.4.2 Timing

Each TDM data line carries eight audio channels. There are up to three lines for input data and up to three lines for output data, depending on the firmware loaded. Input lines are always treated as 24-bit, while output lines can be 24- or 32-bit. The TDM data format and timing is shown in Figure 3.

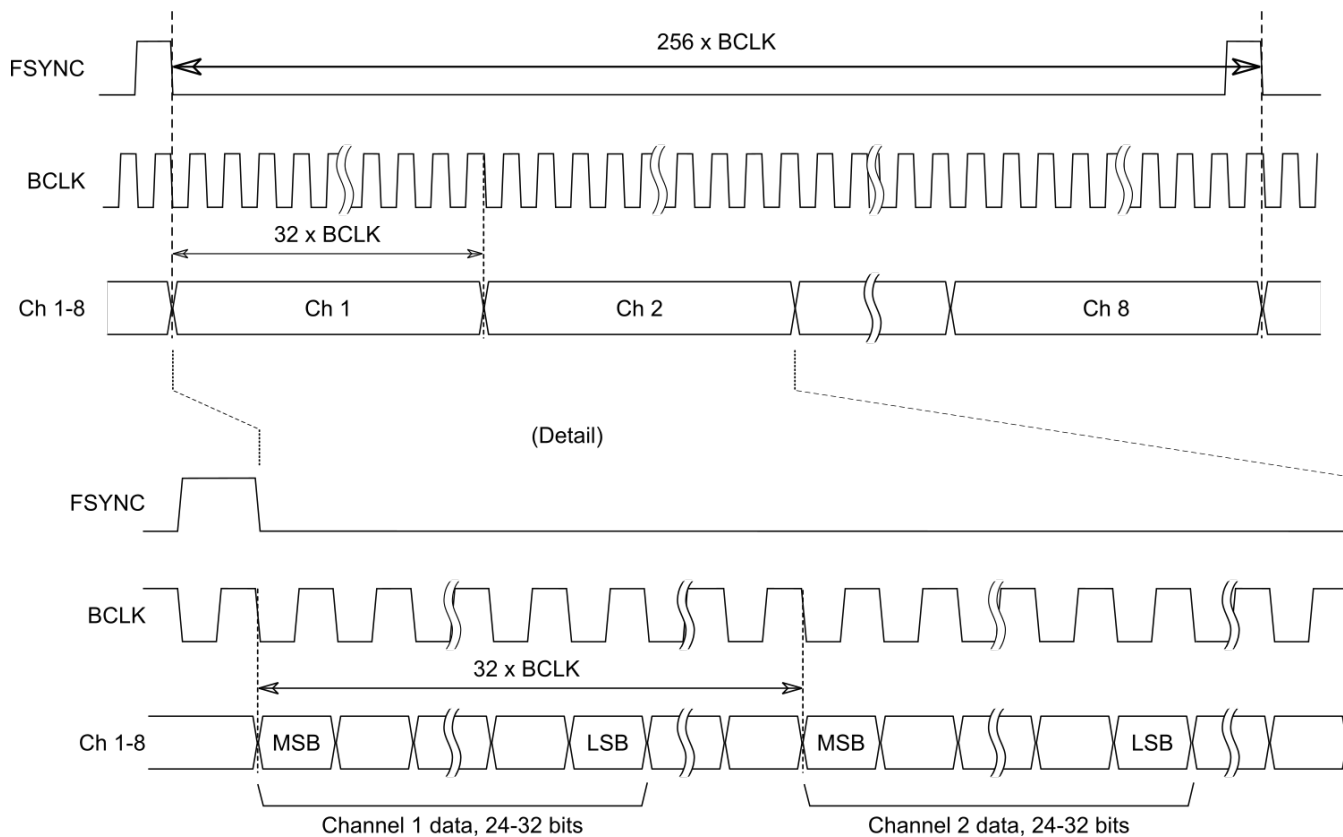


Figure 3. TDM timing

2.5.5 PDM

2.5.5.1 Clocks

PDM has a single clock, which is duplicated on two output lines (PDM_CLK and PDM_CLK2). These clocks are always **outputs**. The connected circuitry must therefore be set to run in slave mode and accept its clocks from the MCHStreamer. (The MCHStreamer always runs as clock master; it cannot be set to run as a clock slave.)

PDM CLK/CLK2 The bit clock. Data for the left channel is taken on the falling edge and data for the right channels taken on the rising edge.

Table 4 summarizes the clocks for the supported effective sample rates. Be sure to double-check that connected circuitry will accept the clocks at the frequencies and ratios listed.

Table 4. PDM clocks

Sample rate	PDM_CLK	PDM_CLK2
8 kHz	3.072 MHz	3.072 MHz
11.025 kHz	2.8224 MHz	2.8224 MHz
16 kHz	3.072 MHz	3.072 MHz
32 kHz	3.072 MHz	3.072 MHz
44.1 kHz	2.8224 MHz	2.8224 MHz
48 kHz	3.072 MHz	3.072 MHz

2.5.5.2 Timing

Each PDM input data line carries two audio channels. The left and right channels are clocked as shown in Figure 4 (only channels 1-4 shown). Input data is always presented to the computer as a 24-bit word. There are eight input data lines, for a total of 16 audio channels.

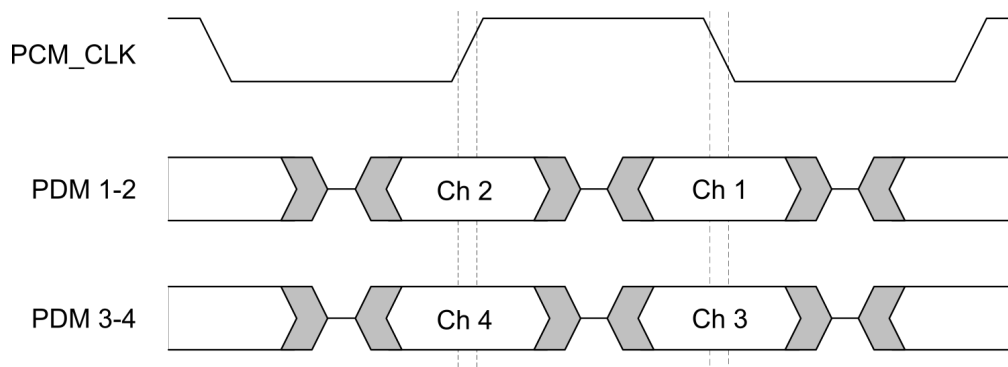


Figure 4. PDM timing

2.5.6 DSD

2.5.6.1 Clocks

DSD has two clock lines. These clocks are always **outputs**. The connected circuitry must therefore be set to run in slave mode and accept its clocks from the MCHStreamer. (The MCHStreamer always runs as clock master; it cannot be set to run as a clock slave.)

MCLK The master clock for both playback and recording. This pin is an output only.

BCLK The bit clock. This clock corresponds to the bit rate of the DSD signal i.e. 64×44100 Hz for DSD64, and so on.

Table 5 summarizes the relation between the clocks. Be sure to double-check that connected circuitry will accept the clocks at the frequencies and ratios listed.

Table 5. DSD clocks

DSD rate	MCLK	BCLK
DSD64	22.5792 MHz	2.8224 MHz
DSD128	22.5792 MHz	5.6448 MHz
DSD256	22.5792 MHz	11.2896 MHz

2.5.6.2 Timing

Each DSD output line carries a single channel modulated at the bit clock rate. The clock and data timing are illustrated in Figure 5 (only channels 1 and 3 shown).

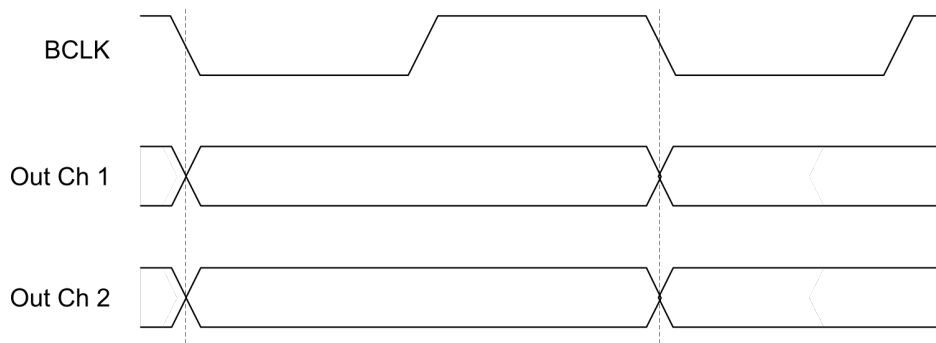


Figure 5. DSD timing

3 FIRMWARE VERSIONS

This section provides the signal flow and pinouts for all firmware files. See Section X for information on loading firmware.

3.1 ALLRATE

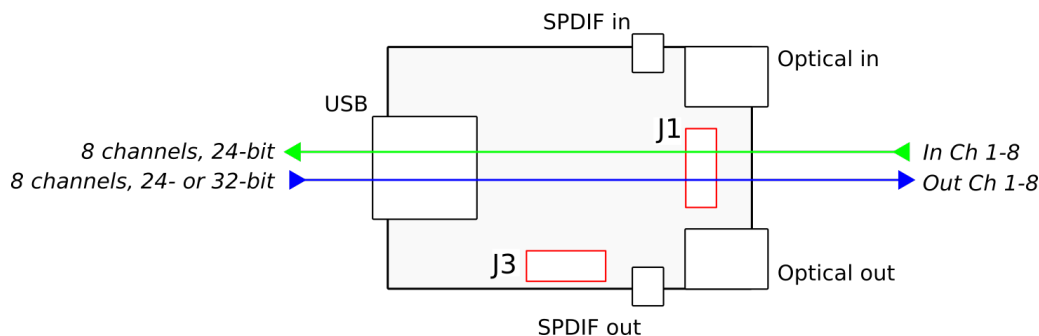


Figure 6. AllRate firmware signal flow

The AllRate firmware supports 8 channels of input and output over I2S. All possible sample rates are supported, from 8 to 384 kHz (see page 27). The optical and SPDIF ports are not used.

Table 6. AllRate firmware pinouts

J1 pin	
1	Out Ch 1-2
2	In Ch 1-2
3	Out Ch 3-4
4	In Ch 3-4
5	Out Ch 5-6
6	In Ch 5-6
7	Out Ch 7-8
8	In Ch 7-8
9	MCLK
10	BCLK
11	GND
12	LRCLK

3.2 TOSLINK_ONLY

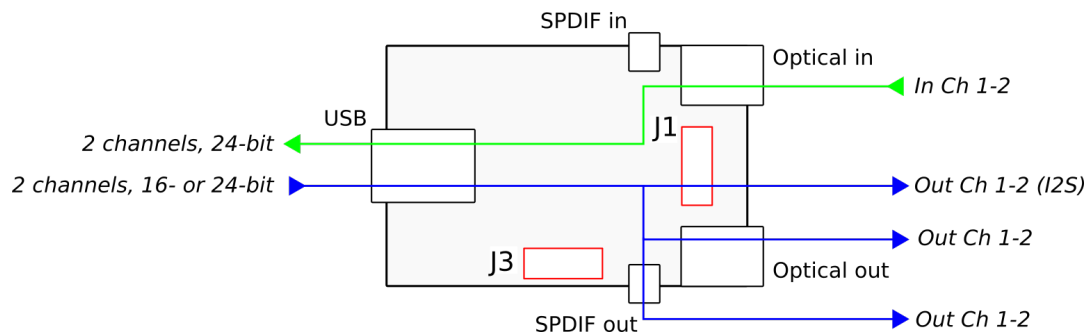


Figure 7. TOSLINK_Only firmware signal flow

The TOSLINK_Only firmware supports two input channels and two output channels at 44.1, 48, 88.2, 96, 176.4 and 192 kHz. The input channels are received on the optical input in SPDIF format and made available to the computer over USB. The two output channels from the computer are sent to J1 (as I2S), the optical output and the SPDIF output.

Table 7. TOSLINK_Only firmware pinouts

J1 pin	
1	Out Ch 1-2
2	—
3	—
4	—
5	—
6	—
7	—
8	—
9	MCLK
10	BCLK
11	GND
12	LRCLK

3.3 SPDIF_ONLY

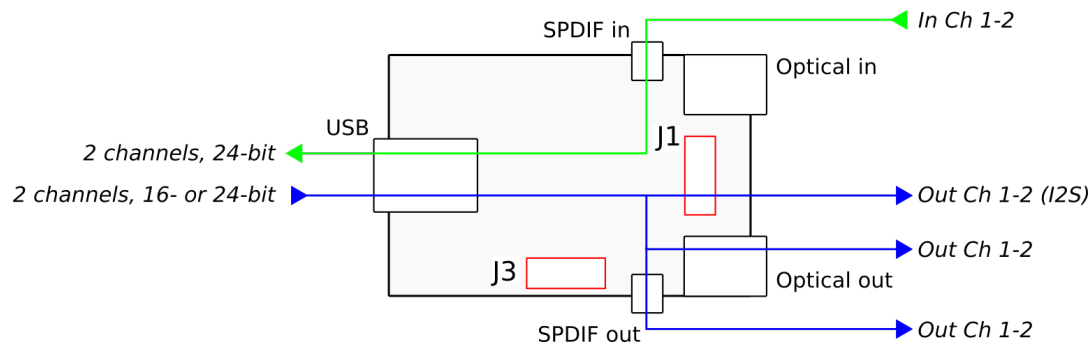


Figure 8. SPDIF_Only firmware signal flow

The SPDIF_Only firmware supports two input channels and two output channels at 44.1, 48, 88.2, 96, 176.4 and 192 kHz. The input channels are received on the SPDIF input and made available to the computer over USB. The two output channels from the computer are sent to J1 (as I2S), the optical output and the SPDIF output.

Table 8. SPDIF_Only firmware pinouts

J1 pin	
1	Out Ch 1-2
2	—
3	—
4	—
5	—
6	—
7	—
8	—
9	MCLK
10	BCLK
11	GND
12	LRCLK

3.4 I2S_TOSLINK

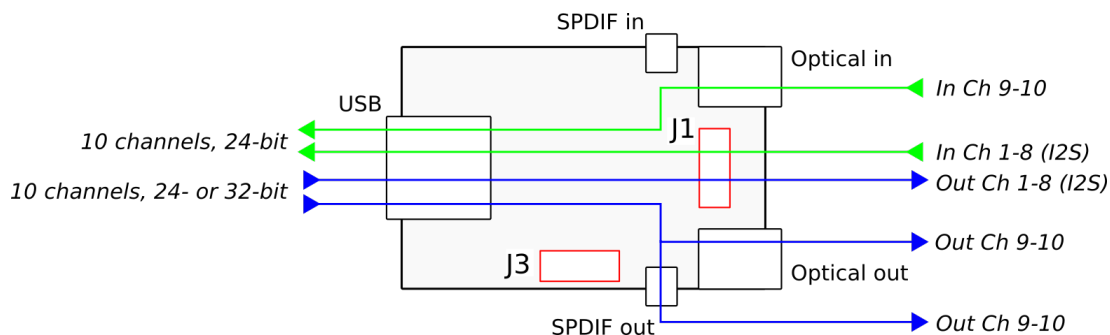


Figure 9. I2S_TOSLINK firmware pinouts

The I2S_TOSLINK firmware supports ten input channels and ten output channels at 44.1, 48, 88.2, 96, 176.4 and 192 kHz. Input channels 1-8 are received on J1 as I2S and input channels 9-10 are received on the optical input in SPDIF format. All ten channels are made available to the computer over USB. Output channels 1-8 from the computer are sent to J1 as I2S while output channels 9-10 are sent to both the optical output and the SPDIF output.

Table 9. I2S_TOSLINK firmware pinouts

J1 pin

1	Out Ch 1-2
2	In Ch 1-2
3	Out Ch 3-4
4	In Ch 3-4
5	Out Ch 5-6
6	In Ch 5-6
7	Out Ch 7-8
8	In Ch 7-8
9	MCLK
10	BCLK
11	GND
12	LRCLK

3.5 I2S_SPDIF

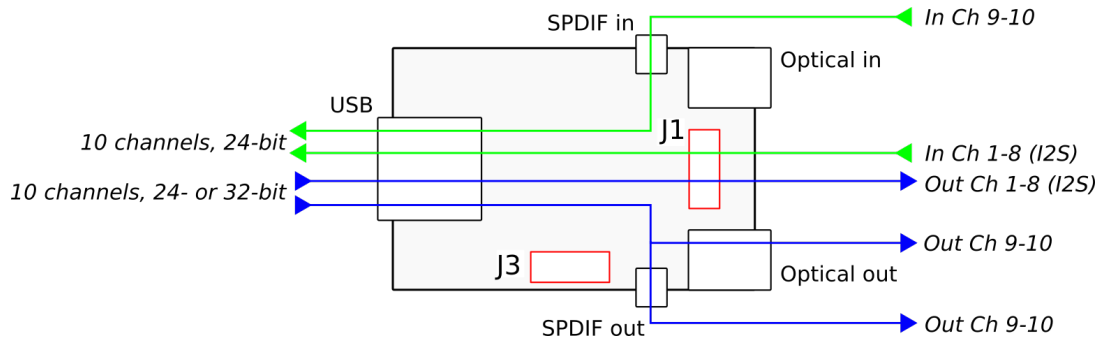


Figure 10. I2S_SPDIF firmware signal flow

The I2S_SPDIF firmware supports ten input channels and ten output channels at 44.1, 48, 88.2, 96, 176.4 and 192 kHz. Input channels 1-8 are received on J1 as I2S and input channels 9-10 are received on the SPDIF input. All ten channels are made available to the computer over USB. Output channels 1-8 from the computer are sent to J1 as I2S while output channels 9-10 are sent to both the optical output and the SPDIF output.

Table 10. I2S_SPDIF firmware pinouts

J1 pin	
1	Out Ch 1-2
2	In Ch 1-2
3	Out Ch 3-4
4	In Ch 3-4
5	Out Ch 5-6
6	In Ch 5-6
7	Out Ch 7-8
8	In Ch 7-8
9	MCLK
10	BCLK
11	GND
12	LRCLK

3.6 ADAT

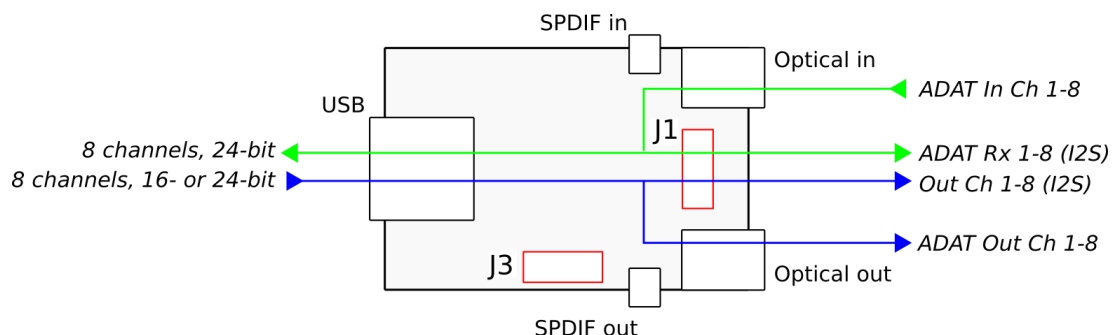


Figure 11. ADAT firmware signal flow

At 44.1 and 48 kHz, the ADAT firmware receives 8 channels on the optical input and mirrors these in I2S format on J1. The inputs are available to the computer over USB. Eight output channels from the computer are transmitted as ADAT on the optical output and as I2S on J1.

At 88.2 and 96 kHz, only 4 channels are received and transmitted. (Although the USB interface will state 8 channels, only the first four can be used.)

Table 11. ADAT firmware pinouts

J1 pin	
1	ADAT Rx 1-2
2	Out 1-2
3	ADAT Rx 3-4
4	Out 3-4
5	ADAT Rx 5-6*
6	Out 5-6*
7	ADAT Rx 7-8*
8	Out 7-8*
9	MCLK
10	BCLK
11	GND
12	LRCLK

* Channels 5 to 8 are active only at 44.1 and 48 kHz.

3.7 TDM

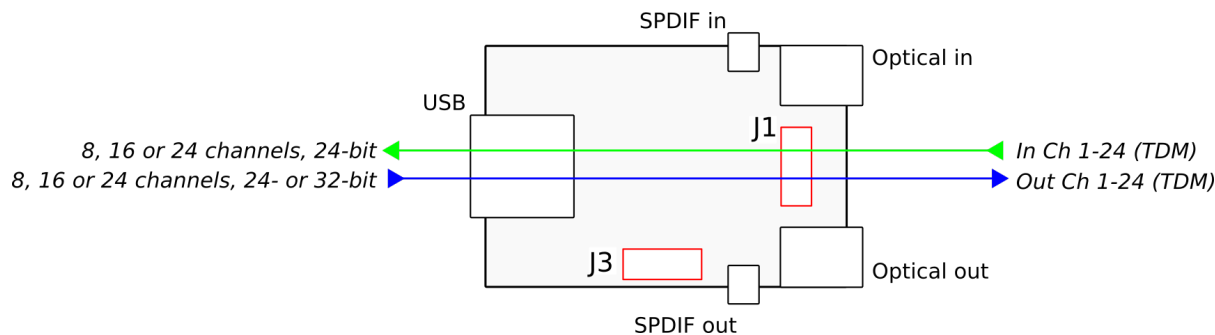


Figure 12. TDM firmware signal flow

The TDM firmware supports 8, 16, or 24 input and output channels at 44.1, 48, 88.1 and 96 kHz. See page 14 for waveforms and clock timing. Each active data line on J1 carries 8 channels. Three different firmware files are provided.

Table 12. TDM firmware pinouts

J1 pin	TDM8	TDM16	TDM24
1	Out Ch 1-8	Out Ch 1-8	Out Ch 1-8
2	In Ch 1-8	In Ch 1-8	In Ch 1-8
3	—	Out Ch 9-16	Out Ch 9-16
4	—	In Ch 9-16	In Ch 9-16
5	—	—	Out Ch 17-24
6	—	—	In Ch 17-24
7	—	—	—
8	—	—	—
9	MCLK	MCLK	MCLK
10	SCLK	SCLK	SCLK
11	GND	GND	GND
12	FSYNC	FSYNC	FSYNC

3.8 PDM

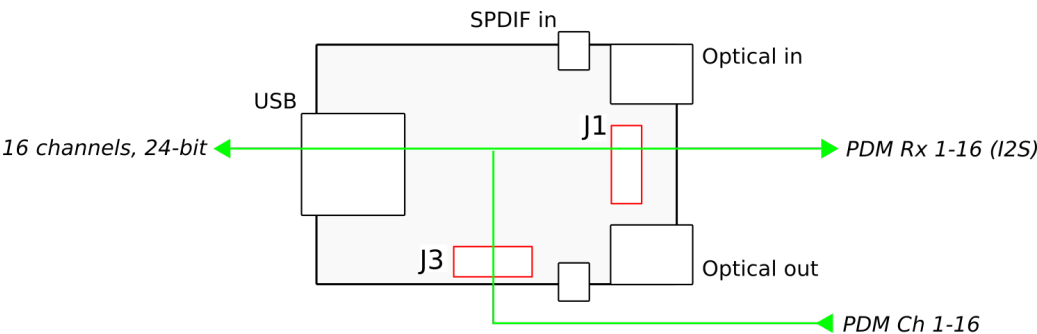


Figure 13. PDM firmware signal flow

The PDM firmware supports 16 input channels at 8, 11.025, 12, 16, 32, 44.1 and 48 kHz. PDM input data is received on J3, with two channels per physical data line as described on page X. These 16 channels are mirrored in I2S format on J1 and are also received by the computer over USB.

Table 13. PDM firmware pinouts

J1 pin		J3 pin	
1	PDM Rx 1-2	1	GND
2	PDM Rx 9-10	2	3.3V
3	PDM Rx 3-4	3	PDM 1-2
4	PDM Rx 11-12	4	PDM 3-4
5	PDM Rx 5-6	5	PDM 5-6
6	PDM Rx 13-14	6	PDM 7-8
7	PDM Rx 7-8	7	PDM 9-10
8	PDM Rx 15-16	8	PDM 11-12
9	MCLK	9	PDM 13-14
10	BCLK	10	PDM 15-16
11	GND	11	PDM CLK
12	LRCLK	12	PDM CLK2

3.9 DSD

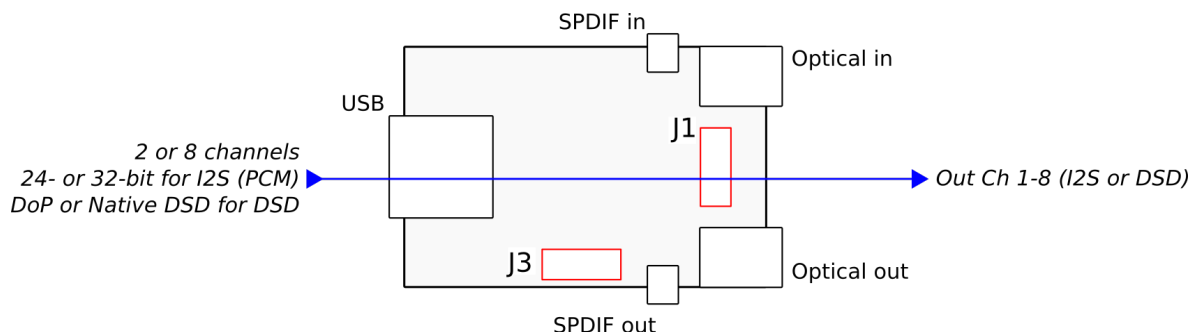


Figure 14. DSD firmware signal flow

There are two versions of the DSD firmware, one supporting stereo output and one supporting 8-channel output. Each operates in two modes: I2S and DSD. If the computer (via the music player program) sends PCM data, PCM data in I2S format is output on J1 (see page 12). As usual for I2S, two channels are multiplexed onto each physical pin. In PCM mode, sample rates from 44.1 to 384 kHz are supported.

If the computer (via the music player program) sends DSD data either in DoP (DSD over PCM) or native DSD format, then bitstream outputs are provided on J1, with each physical pin carrying only a single channel (see page 17). In DSD mode, DSD64, DSD128 and DSD256 rates are supported. On Windows, the music player program will typically have a setting to enable either DoP or DSD bitstream output via the miniDSP ASIO driver. On Mac, native DSD is not supported, so the music player will need to be set to send DoP when playing DSD files.

The PCM/DSD pin is used to warn the DAC which mode it operates (PCM or DSD mode)

Table 14. DSD firmware pinouts

J1 pin	PCM mode		DSD mode	
	0i2o_DSD	0i8o_DSD	0i2o_DSD	0i8o_DSD
1	Out Ch 1-2	Out Ch 1-2	Out Ch 1	Out Ch 2
2	—	—	—	Out Ch 6
3	—	Out Ch 3-4	Out Ch 2	Out Ch 3
4	—	—	—	Out Ch 7
5	—	Out Ch 5-6	—	Out Ch 4
6	—	—	—	Out Ch 8
7	—	Out Ch 7-8	—	Out Ch 5
8	PCM/DSD Pin: Logic 0 (LOW)		PCM/DSD Pin: Logic 1 (HIGH)	
9	MCLK	MCLK	MCLK	MCLK
10	BCLK	BCLK	BCLK	BCLK
11	GND	GND	GND	GND
12	LRCLK	LRCLK	—	Out Ch 1

3.10 SAMPLE RATE SUMMARY

Sample Rate	SPDIF_Only	TOSLINK_Only	I2S_SPDIF	I2S_TOSLINK	ADAT	TDM 8	TDM 16	TDM 24
44100	Y	Y	Y	Y	Y	Y	Y	Y
48000	Y	Y	Y	Y	Y	Y	Y	Y
88200	Y	Y	Y	Y	Y ¹	Y	Y	Y
96000	Y	Y	Y	Y	Y ¹	Y	Y	Y
176400	Y	Y	Y	Y				
192000	Y	Y	Y	Y				

Sample Rate	AllRate	0i2o_DSD (PCM)	0i8o_DSD (PCM)	0i2o_DSD (DSD)	0i8o_DSD (DSD)	PDM
8000	Y					Y
11025	Y					Y
12000	Y					Y
16000	Y					Y
32000	Y					Y
44100	Y	Y	Y			Y
48000	Y	Y	Y			Y
88200	Y	Y	Y			
96000	Y	Y	Y			
176400	Y	Y	Y			
192000	Y	Y	Y			
352800	Y	Y	Y			
384000	Y	Y	Y			
DSD64				Y	Y	
DSD128				Y	Y	
DSD256				Y ²	Y ²	

¹ 4 channels only at 88.2 and 96 kHz.

² DSD256 is supported for native DSD only. DoP (DSD over PCM) is not supported for this rate.

4 INSTALLATION AND CONFIGURATION – WINDOWS

Please read and follow all steps in this section carefully.

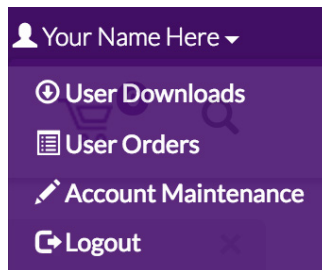
4.1 DOWNLOAD

If you purchased your product directly from miniDSP, your software will be available from the [User Downloads](#) section of the miniDSP website when your order ships. You will need to be logged into the website with the account you created when purchasing to access the download.

If you purchased your product from a miniDSP dealer, you will receive a coupon together with the product. Redeem this coupon and select the Plugin Group “USBStreamer... Drivers” at the link below:

- <https://www.minidsp.com/support/redeem-coupon>

The User Downloads link is visible from the dropdown menu at the top right of the website page:



Navigate to the **USB Audio Drivers** section and download the zip file under the heading **MCHStreamer drivers**. Unzip the downloaded file by right-clicking on it and selecting “Extract All...”.

4.2 USB DRIVER INSTALLATION

The USB driver enables Windows to stream audio to the MCHStreamer. In addition, it installs a control panel to help manage the MCHStreamer, and the firmware updater necessary to load the most suitable firmware version.

To install the driver, the MCHStreamer **must** be connected to the computer by USB. Go to the **WinDrivers** folder of the installation download and double-click on the appropriate installer:

- **miniDSP_UAC2_v2.29.3_ForWinXP_Vista.exe** for Windows XP and Vista
- **miniDSP_UAC2_v4.47.0_ForWin7_8_10.exe** for Windows 7, 8, and 10

(The version number embedded in the filename may be different.)

We recommend accepting the default installation location. Once the driver installation completes, click the **Finish** button.



The Windows PC will not be able to communicate properly with the MCHStreamer if you did not have the MCHStreamer connected by USB when you ran the installer. If that is the case, you will need to uninstall the driver, connect the MCHStreamer and run the installer again.

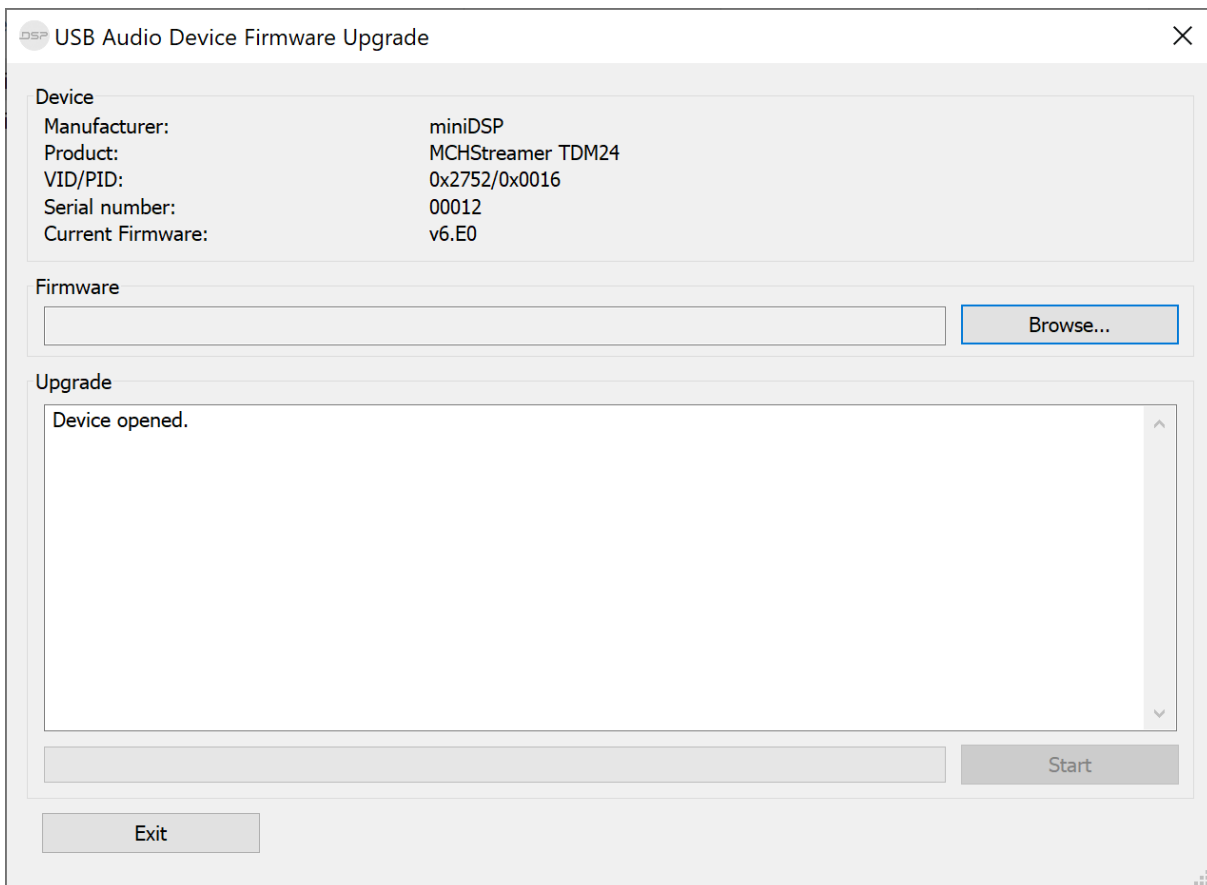
4.3 LOADING FIRMWARE

If the default firmware loaded into your MCHStreamer as shipped is not suited for your application, you will need to load a different firmware version. (You do not need to load firmware if the default firmware is suitable for your application.)

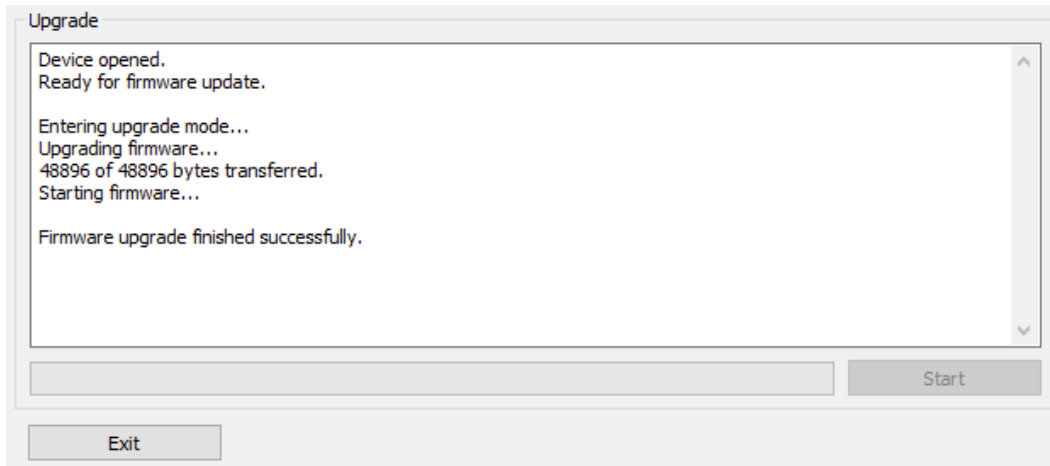
- MCHStreamer B (box) has ADAT firmware loaded when shipped.
- MCHStreamer kit has the I2S_TOSLINK firmware loaded when shipped.

To load a different firmware version:

1. Connect the MCHStreamer to your computer via USB (if not already connected).
2. Navigate to the **Firmware\Firmware_Upgrade_Tools\Windows\miniDSPUAC2Dfu** folder of the software download.
3. Double-click on the **miniDSPUAC2Dfu.exe** program to run it:



4. Click on the **Browse** button and navigate to the plugin download folder and then the **Firmware** folder. Select the most suitable firmware file according to your application. See Section 3.
5. Click on the **Start** button.
6. You will get a progress bar as upgrade proceeds. When it completes, you will see a message that the upgrade completed successfully:

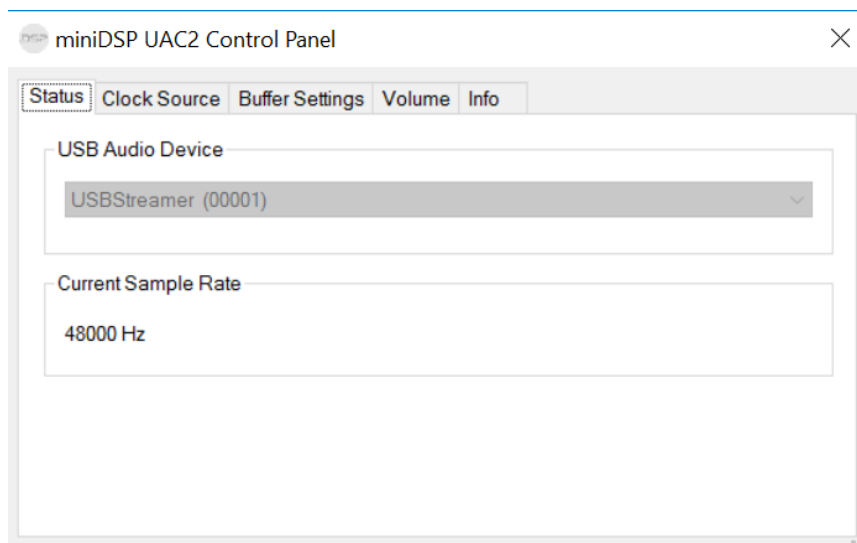


7. Click on **Exit**.
8. That's it! You're done. You can now use your MCHStreamer with the new firmware.

4.4 MCHSTREAMER CONTROL PANEL

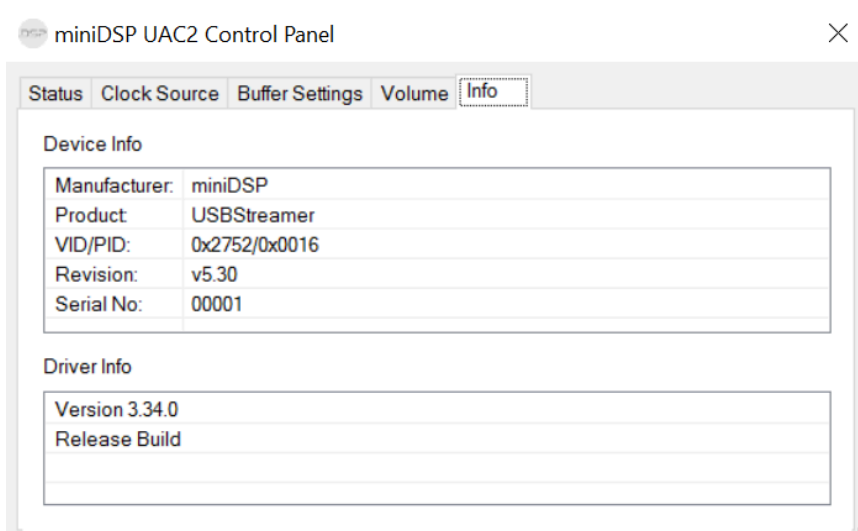
To configure the MCHStreamer, open the **miniDSP UAC2 Control Panel** (from Start Menu -> miniDSP Ltd). It has several tabs.

The status pane shows the current sample rate of the MCHStreamer. This setting cannot be changed in the Control panel, but simply reflects the current sample rate of the MCHStreamer.



4.4.1 Info

This pane shows information about the MCHStreamer.



5 INSTALLATION AND CONFIGURATION – MAC OS X

Mac OS X has native support for USB Audio class 2.0 devices, so no driver installation is required. However, you will most likely need to download the software package to install the correct firmware for your application.

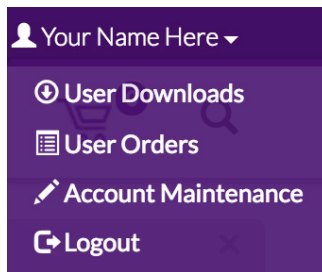
5.1 DOWNLOAD

If you purchased your product directly from miniDSP, your software will be available from the [User Downloads](#) section of the miniDSP website when your order ships. You will need to be logged into the website with the account you created when purchasing to access the download.

If you purchased your product from a miniDSP dealer, you will receive a coupon together with the product. Redeem this coupon and select the Plugin Group “USBStreamer... Drivers” at the link below:

- <https://www.minidsp.com/support/redeem-coupon>

The User Downloads link is visible from the dropdown menu at the top right of the website page:



Navigate to the **USB Audio Drivers** section and download the zip file under the heading **MCHStreamer drivers**. Unzip the downloaded file by double-clicking on it.

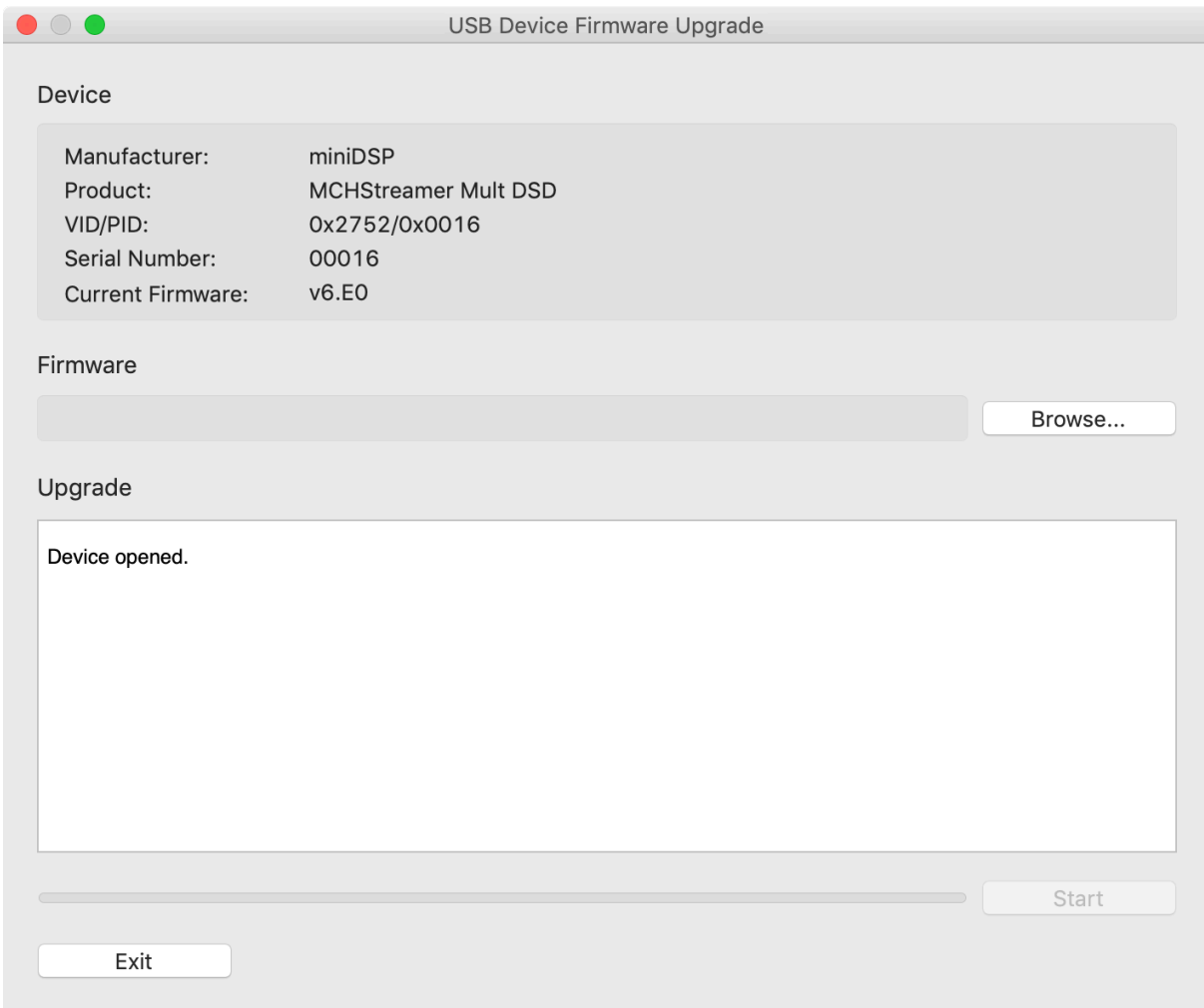
5.2 LOADING FIRMWARE

If the default firmware loaded into your MCHStreamer as shipped is not suited for your application, you will need to load a different firmware version. (You do not need to load firmware if the default firmware is suitable for your application.)

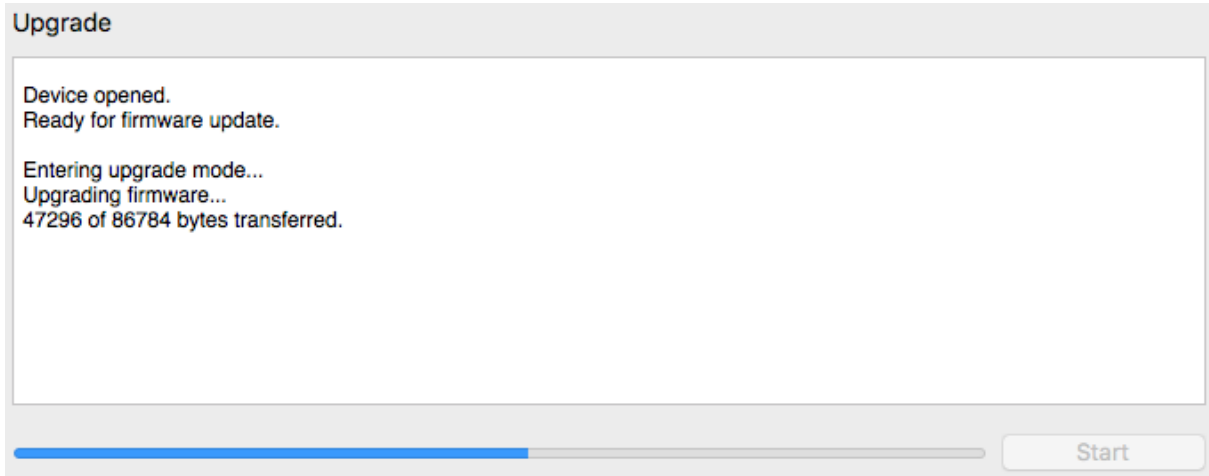
- MCHStreamer B (box) has ADAT firmware loaded when shipped.
- MCHStreamer Kit has TOSLINK/I2S firmware loaded when shipped.

To load firmware:

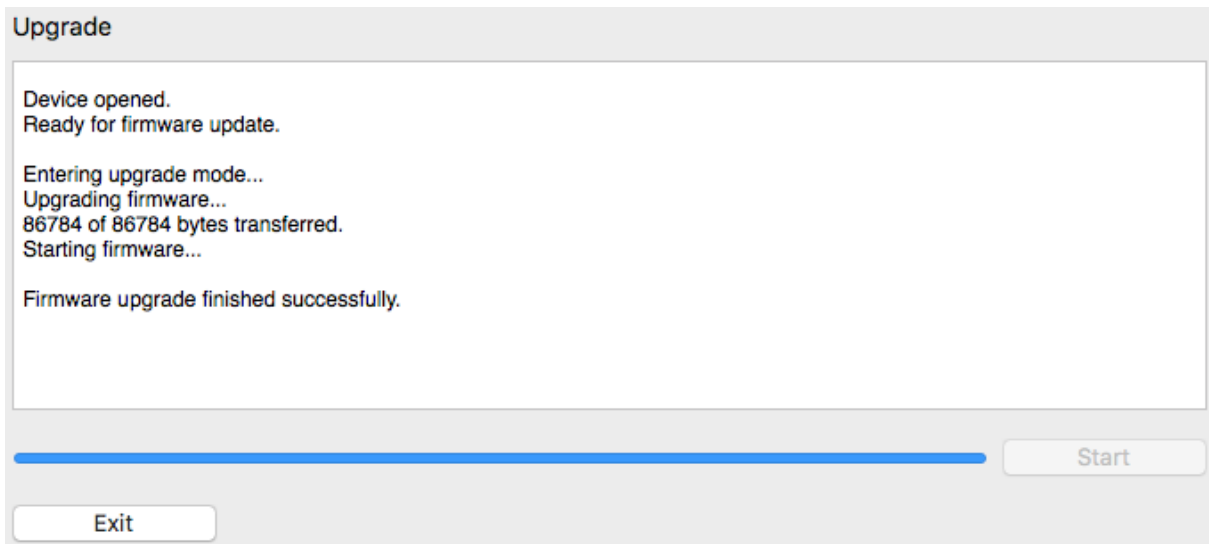
1. Connect the MCHStreamer to your computer via USB (if not already connected).
2. Navigate to the **Firmware/Firmware_Upgrade_Tools/Mac** folder of the software download.
3. Double-click on the **DFU Utility.app** program to run it:



4. Click on the **Browse** button and navigate to the plugin download folder and then the **Firmware** folder. Select the most suitable firmware file according to your application. See Section 3.
5. Click on the **Start** button.
6. You will get a progress bar as the upgrade proceeds:



7. Once the firmware upgrade completes, you will see a message that the upgrade completed successfully:



8. Click on **Exit**.
9. That's it! You're done. You can now use your MCHStreamer with the new firmware.

6 ADDITIONAL INFORMATION

6.1 SPECIFICATIONS

Computer connectivity	USB 2.0, USB Audio Class 2 compliant
Driver	Mac OS X: no driver required Windows: driver provided
Audio resolution and sample rate	See Section 3 of this manual.
Enclosure	Aluminum, sand blasted and anodized (MCHStreamer B only)
Power supply	USB-powered. Optional 5VDC power supply on 12-pin header J2.
Dimensions (H x W x D)	13 x 40 x 62 mm (MCHStreamer) 24 x 64 x 67.4 mm (MCHStreamer B)

6.2 OBTAINING SUPPORT

1. Check the forums on minidsp.com to see if this issue has already been raised and a solution or solutions provided.
2. Contact miniDSP via the support portal at support.minidsp.com with:
 - a. The product information including OS version and version of driver installed (for Windows).
 - b. A clear explanation of the symptoms you are seeing.
 - c. A description of the troubleshooting steps you performed and the results obtained.